Atty. Dkt. No. 300204380-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: John Deryk WATERS

Title: MEMORY TAG

Appl. No.: Unassigned

Filing Date: 10/31/2003

Examiner: Unassigned

Art Unit: Unassigned

CLAIM FOR CONVENTION PRIORITY

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

The benefit of the filing date of the following prior foreign application filed in the following foreign country is hereby requested, and the right of priority provided in 35 U.S.C. § 119 is hereby claimed.

In support of this claim, filed herewith is a certified copy of said original foreign application:

- Great Britain Patent Application No. 0227203.7 filed 11/21/2002.

Respectfully submitted,

Date: October 31, 2003

By ______________________

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Customer Number: 22879

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Attorney for Applicant
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002.1100505.1

The Patent Office

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Concept House
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Newport
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NP10 8QQ

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Signed R. Mahoney

Dated 8 October 2003

Patents Form 1/77

Patents Act 1977
(Rule 16)

1/77

21NOV02 E765325-1 D01463
P01/7700 0.00-0227203.7

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
South Wales
NP10 8QQ

1. Your reference — 300204380-1 GB

2. Patent application number *(The Patent Office will fill in this part)* — 21 NOV 2002 — 0227203.7

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*
   Hewlett-Packard Company
   3000 Hanover Street
   Palo Alto
   CA 94304, USA

   00496588001
   Patents ADP number *(if you know it)*

   If the applicant is a corporate body, give the country/state of its incorporation — Delaware, USA

4. Title of the invention — Memory Tag

5. Name of your agent *(if you have one)*
   "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*
   Richard A. Lawrence
   Hewlett-Packard Ltd, IP Section
   Filton Road, Stoke Gifford
   Bristol BS34 8QZ

   Patents ADP number *(if you know it)* 07448038001

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*
   a) any applicant named in part 3 is not an inventor, or
   b) there is an inventor who is not named as an applicant, or
   c) any named applicant is a corporate body.
   See note (d))

   Yes

Title: Memory Tag

Field of the Invention

This invention relates to a memory tag, and a reader.

Background of the Invention

Memory tags in the form of Radio Frequency Identification (RFID) tags are well known in the prior art, and the technology is well established (see for example: RFID Handbook, Klaus Finkenzeller, 1999, John Wiley & Sons). RFID tags come in many forms but all comprise an integrated circuit with information stored on it and a coil which enables it to be interrogated by a read/write device generally referred to as a reader. Until recently RFID tags have been quite large, due to the frequency they operate at (13.56MHz) and the size of coil they thus require, and have had very small storage capacities. Such RFID tags have tended to be used in quite simple applications, such as for file tracking within offices or in place of or in addition to bar codes for product identification and supply chain management.

Much smaller RFID tags have also been developed, operating at various frequencies. For example Hitachi-Maxell have developed "coil-on-chip" technology in which the coil required for the inductive link is on the chip rather than attached to it. This results in a memory tag in the form of a chip of 2.5mm square, which operates at 13.56MHz. In addition Hitachi has developed a memory tag referred to as a "mu-chip" which is a chip of 0.4mm square and operates at 2.45GHz. These smaller memory tags can be used in a variety of different applications. Some are even available for the tagging of pets by implantation.

Although it is known to provide tags with their own power source, in many applications the tag is also powered by the radio frequency signal generated by the reader. Such a known system is shown in Figure 1 where a reader is indicated generally at 10 and a tag at 12. The reader 10 comprises a radio frequency generator 13 and a resonant circuit part 11, in the present

voltage drop across the reader inductor 14. Thus, by controlling the switch 23, data stored in the memory 18 of the tag 12 can be transmitted to the reader 10.

A problem in transmitting data from the tag in this manner arises because the memory 18 is also powered by energy drawn from the electromagnetic field of the reader 10. Thus, when the switch 23 is closed, the power source supplying the rectifying circuit 17 is effectively shorted out. Although variations in the voltage at the memory 18 will be to some extent be smoothed by the capacitor 22, there will nevertheless be undesirable voltage changes at the memory 18, necessitating the addition of power control circuitry.

An aim of the invention is to provide a tag which reduces or overcomes this problem.

Summary of the Invention

According to a first aspect of the invention, we provide a memory tag responsive to a signal generated by a reader, the tag comprising a resonant circuit part having a resonant frequency, the resonant frequency of the resonant circuit part being variable in accordance with data to be transmitted to transmit data to the reader.

The resonant circuit part may comprise a variable capacitance element, the capacitance of the variable capacitance element being controllable to vary the resonant frequency of the resonant circuit part.

The resonant circuit part may comprise an inductor and a first capacitor, and wherein the variable capacitance element comprises a second capacitor connected in parallel with the first capacitor and in series with a switch operable to switch the second capacitor element out of the circuit.

The switch may comprise a field effect transistor.

The resonant circuit part may comprise an inductor, and the variable capacitance element may comprise a varactor diode connected in parallel with the inductor and wherein a control line is connected to the cathode of the varactor diode to vary the reverse bias voltage of the varactor diode.

comprise the step of varying the capacitance of the variable capacitance element.

According to a fourth aspect of the invention, we provide a method of reading data from a memory tag, the method comprising the step of supplying a driving signal to a resonant circuit part of a reader, comparing a reference signal corresponding to the driving signal and a reflected signal reflected from the resonant circuit part, and detecting the relative phase of the reference signal and the reflective signal.

The step of comparing the reflected signal and the reference signal may comprise multiplying the reflected signal and the reference signal, and passing the resulting signal through a low pass filter, wherein the output of the load pass filter is dependent on the relative phase.

Brief Description of the Drawings

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings, wherein;

Figure 1 is a schematic circuit diagram of a tag and reader of known type,

Figure 2 is a diagrammatic illustration of a circuit for a tag and reader embodying the present invention,

Figure 3a is a diagrammatic circuit diagram of a further tag embodying the present invention,

Figure 3b is a diagrammatic illustration of a yet further tag embodying the present invention,

Figure 4a is a graph showing variation in the amplitude of a reflected signal detected by the reader,

Figure 4b is a graph showing variation in the phase of a reflected signal detected by the reader, and

Figure 5 is a graph showing data transmitted by the tag of Figure 2 and an output voltage requested by a rectifying circuit of the tag of Figure 2.

The inductor L1 43 comprises an antenna of the reader 31, and the inductor 35 comprises an antenna of the tag 30.

The reference signal from the splitter 47 will be of the form

$$S(t)=A\cos(\omega t)$$

and the reflected signal R(t) tag will be of the form

$$R(t)=\underline{a}\cos(\omega t+\varphi(t))$$

where

A = amplitude of the reference signal,

a = amplitude of the reflected signal

$\varphi(t)$ = the relative phase and

ω = the frequency of the signal generated by the frequency source 45.

R(t) is multiplied by the carrier reference signal S(t) at the multiplier 49, producing a resulting signal

$$\frac{aA}{2}\cos(2\omega t+\varphi(t))+\frac{aA}{2}\cos(\varphi(t))$$

The first of these terms, the second harmonic, is simply filtered by the low pass filter 50 leaving the second term that comprises the phase difference between the reference and reflected signals. It is a known effect of resonant circuits that when the circuit passes a signal which has a frequency less than the resonant frequency of the resonant circuit, a phase lag is introduced to the passed signal frequency, whilst when the frequency is greater than that of the resonant circuit,

closed as shown in Figure 3a, the DC supply generated in the tag will be generally constant and stable, as shown in the top plot of Figure 5c.

Two possible implementations of the variable capacitance device 37 are shown in Figure 3a and 3b. In Figure 3a, the switch 37 is provided by an transistor 37′, in this case a field effect transistor (FET) controlled by a control line 34a to the memory 34 and connected to the gate of the FET. In the alternative of Figure 4b, the switch 37 is provided by a varactor diode 37″ connected with its cathode connected to the memory 34 via control line 34a. The control line 34a′ is provided with a resistor R1 34b. Since the varactor diode 37″ is only required to be reverse-biased, the resistor R1 34b can be of a relatively high resistance. This high resistance then prevents any RF energy at the varactor cathode entering the memory 34. A characteristic of a varactor diode is that the capacitance falls with increasing reverse bias. Thus when a relatively high voltage is supplied to the cathode of the varactor diode 37″ via the control line 34a′, its capacitance will be relatively low and thus the resonant frequency of the resonant circuit part will be relatively high. When no voltage is applied to the cathode of the varactor diode 37″, its capacitance will be relatively high and the resonant frequency of the resonant circuit part will be relatively low. Of course, it will be apparent that the varactor diode 37″ may be used to modulate the resonant frequency of the resonant circuit of 32 and thus the detected phase between multiple levels, or even in an analogue fashion as required.

In a preferred embodiment, the resonant frequency of the resonant circuit part 42, and hence the frequency of the signal generated by the frequency source 45 is about 2.45 GHz, and the resonant frequency of the resonant circuit part 32 is modulated by about 0.05 GHz either side of this reference frequency. At this frequency, component values for the inductors and the capacitors are small, allowing easy integration of the circuit and require relatively small areas of silicon on an integrated circuit. It is particularly

CLAIMS

1. A memory tag responsive to a signal generated by a reader, the tag comprising a resonant circuit part having a resonant frequency, the resonant frequency of the resonant circuit part being variable in accordance with data to be transmitted being variable to transmit data to the reader.

2. A memory tag according to claim 1 wherein the resonant circuit part comprises a variable capacitance element, the variable capacitance element being controllable to vary the resonant frequency of the resonant circuit part.

3. A memory tag according to claim 2 wherein the resonant circuit part comprises an inductor and a first capacitor, and wherein the variable capacitance element comprises a second capacitor connected in parallel with the first capacitor and in series with a switch operable to switch the second capacitor element out of the circuit.

4. A memory tag according to claim 3 wherein the switch comprises a field effect transmitter.

5. A memory tag according to claim 2 wherein the resonant circuit part comprises an inductor and wherein the controllable capacitive element comprises a varactor diode connected in parallel with the inductor and wherein a control line is connected to the cathode of the varactor diode to vary the reverse bias voltage of the varactor diode.

6. A memory tag according to claim 5 wherein the resonant circuit part comprises a first capacitor connected in parallel with the inductor.

14. A reader substantially as descried herein and/or with reference to the accompanying drawings.

15. A method of transmitting data from a memory tag to a reader, wherein the tag comprises a resonant circuit part having a resonant frequency, the method comprising the step of varying the resonant frequency of the resonant circuit part to transmit data to the reader.

16. A method according to claim 15 wherein the resonant circuit part comprises a variable capacitance element, and the step of varying the resonant frequency of the resonant circuit part comprising the step of varying the capacitance of the variable capacitance element.

17. A method of reading data from a memory tag, the method comprising the step of supplying a driving signal to a resonant circuit part of a reader, the method comprising the step of comparing a reference signal corresponding to the driving signal and a reflected signal reflected from the resonant circuit part, and detecting the relative phase of the reference signal and the reflective signal.

18. A method according to claim 17 wherein the step of comparing the reference signal and the reflected signal comprises the steps of multiplying the reflected signal and the reference signal, and passing the resulting signal through a low pass filter, wherein the output of the load pass filter is dependent on the relative phase.

19. A method substantially as described herein, and/or with reference to the accompanying drawings.

ABSTRACT

Title: Circuit

A memory tag responsive to a signal generated by a reader, the tag comprising a resonant circuit part having a resonant frequency, the resonant frequency of the resonant circuit part being variable in accordance with data to be transmitted being variable to transmit data to the reader.

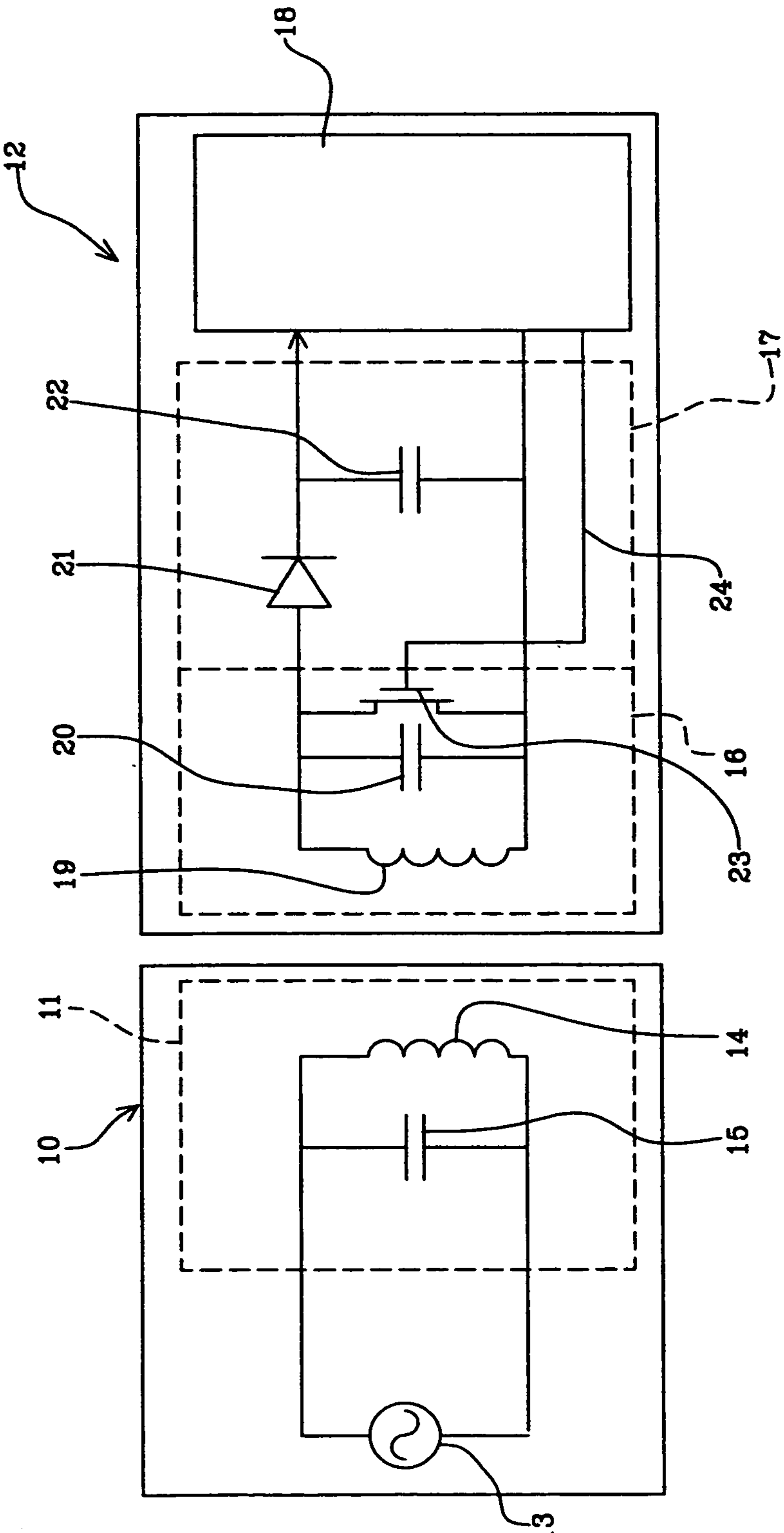
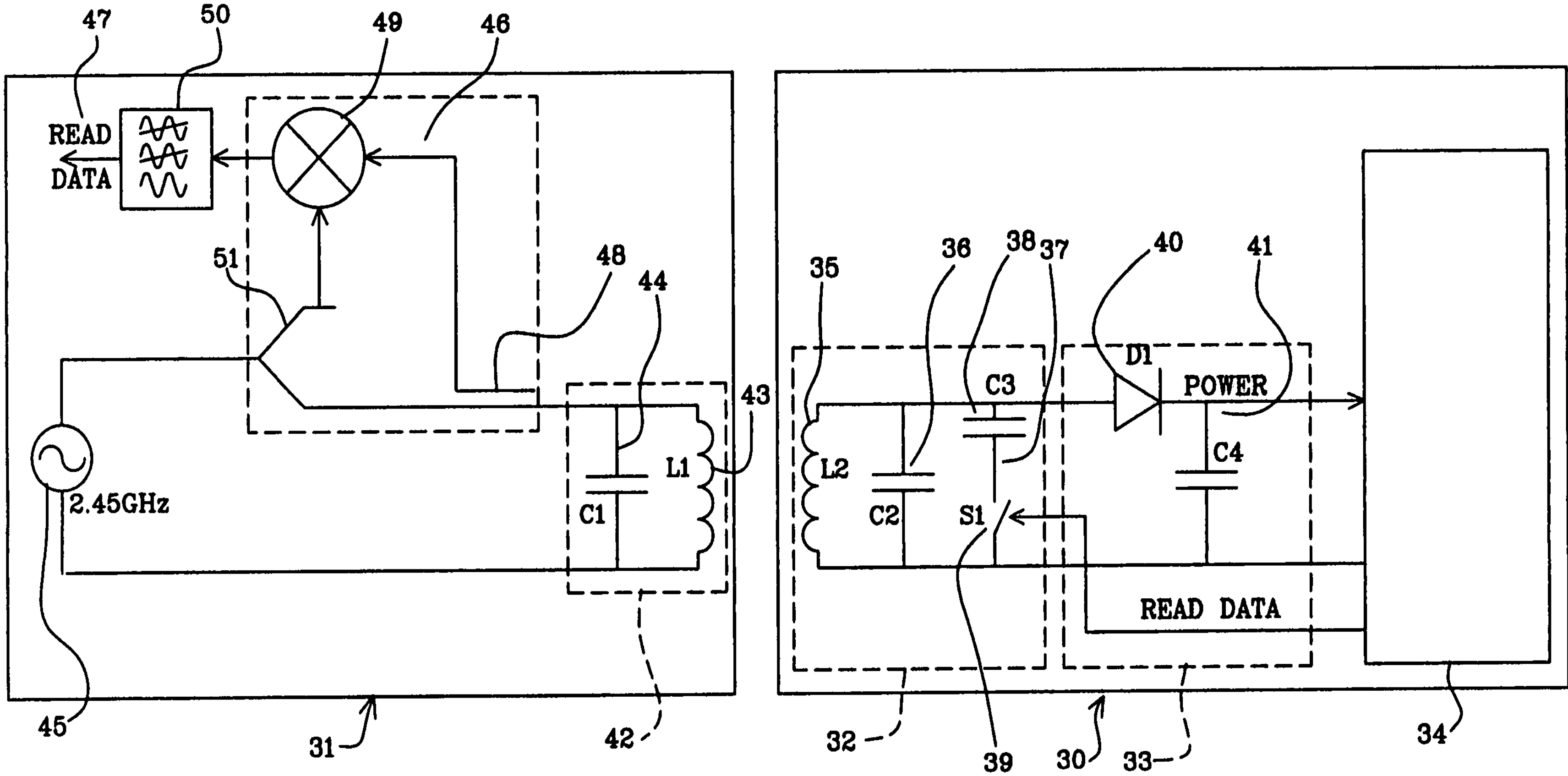


FIG 1(prior art)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DATA
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48
44
43
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C1
2.45GHz
45
31
42
35
36
38
37
40
41
D1
POWER
C3
C4
L2
C2
S1
READ DATA
32
39
30
33
34

FIG 2

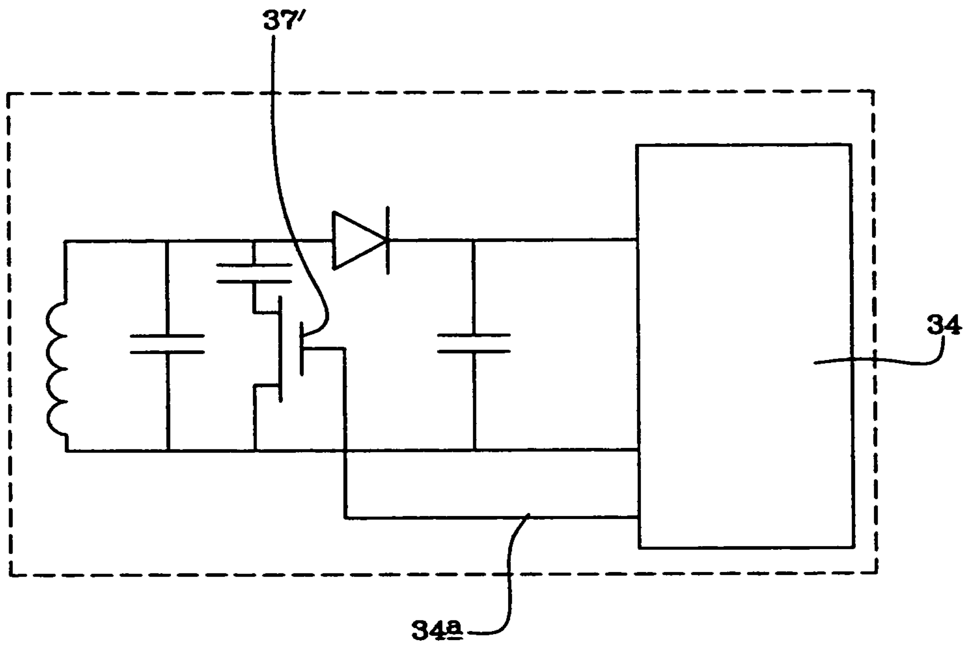


FIG 3a

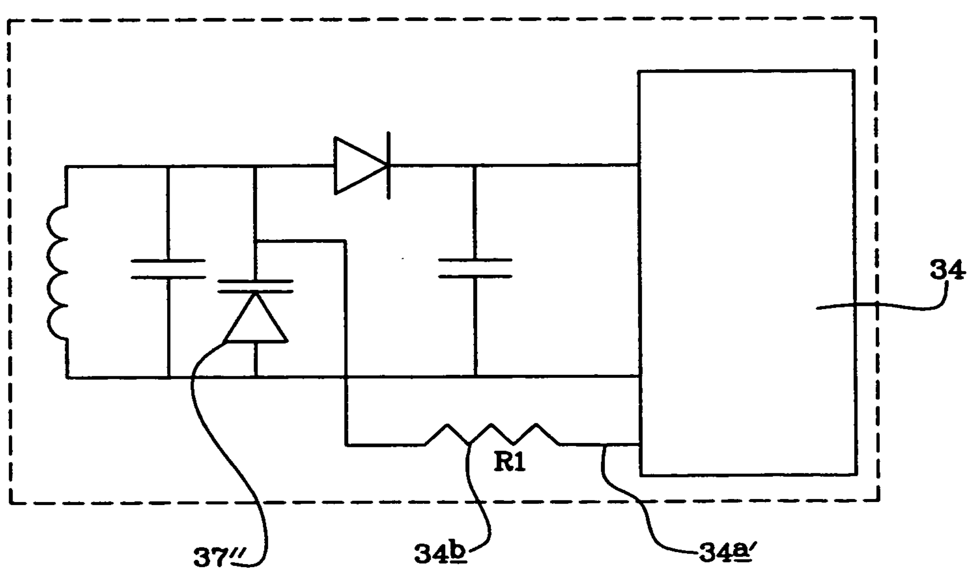
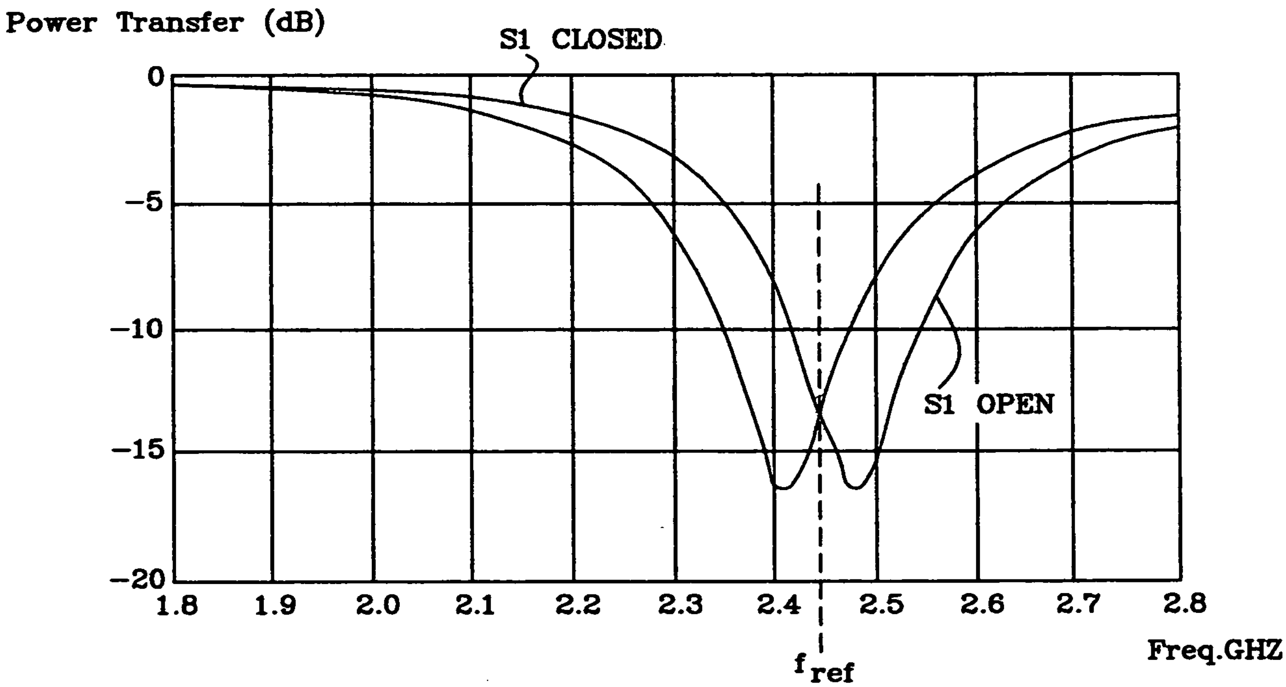


FIG 3b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0
-5
-10
-15
-20
1.8
1.9
2.0
2.1
2.2
2.3
2.4
2.5
2.6
2.7
2.8
S1 OPEN
Freq.GHZ
f_{ref}

FIG 4a

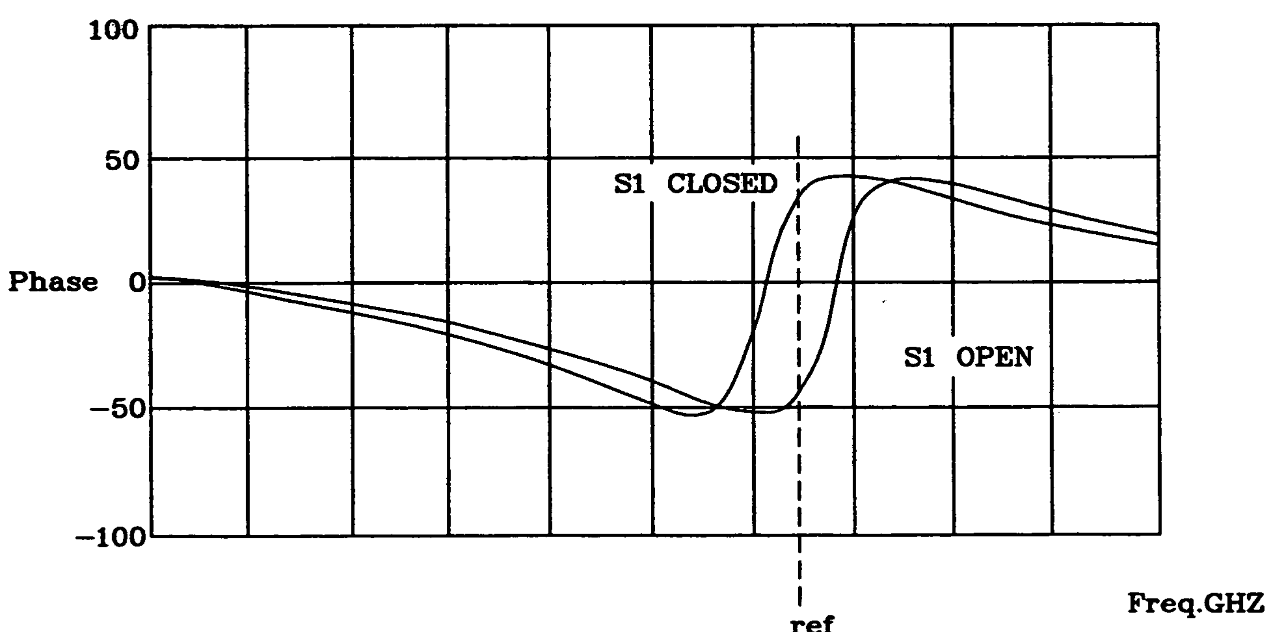
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FIG 4b

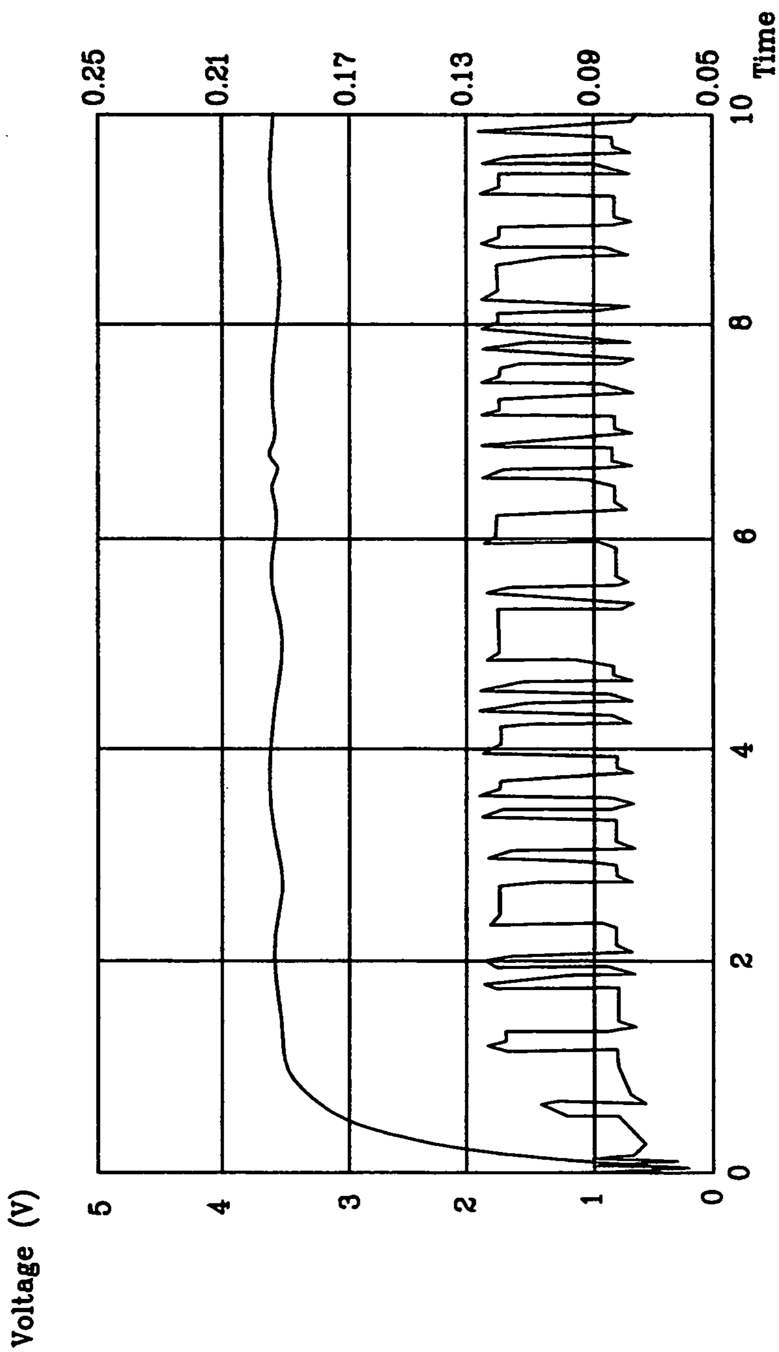

FIG 5